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TITLE: Device for enhancing the performance of a real time executive kernel associated with a multiprocessor structure that can include a large number of processors
DATE-ISSUED: March 15, 1994

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
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CLAIMS:

There is claimed:
1. Device for optimizing the performance of a real time executive kernel in a multiprocessor structure comprising one or more processors, said device comprising a real time operator behaving, as seen from a processor of said structure, as a memory area and comprising means for sending and for receiving data to be processed, means for generating communication control signals, means for associating with objects managed by a kernel, especially tasks, each having a state, hardware and software events, resources and time, a series of primitives one primitive at a time to manage a clock resource and active resources, means for managing a real time context of said processors of said structure on the basis of a predetermined strategy by means of a scheduler, said scheduler being adapted in particular to activate the tasks cyclically, means for marking waits on timers, means for activating tasks after timers, and means for deciding to change the state of a task to another state on the basis of the primitives of the real time context, wherein said real time operator is organized in a plurality of identical hardwired real time operator circuits, accessible simultaneously by said processors of said structure but each associated with one only of said processors, said circuits being interconnected by a link adapted to transmit an "AGREED" signal ensuring that said real time operator executes only one primitive at a time, each real time operator circuit comprising a scheduler which manages the tasks of only the processor associated with it and global resources and events of the real time operator, said scheduler comprising means for activating the tasks cyclically, means for marking waits on timers and means activitating tasks after timers, said real time operator deciding to change the task state on the basis of primitives of the real time context, said device comprising means for commuting each real time operator circuit in one of the following three functioning modes:
a) a first mode in which it processes a primitive requested by one of said processors of said structure,
b) a second mode in which it processes a local request internal to the circuit concerning only tasks for which it is responsible,

c) a third mode in which it is awaiting processing.
2. Device according to claim 1 wherein said real time operator comprises means for processing one of said primitives only if all said real time operator circuits are awaiting processing.
3. Device according to claim 1, wherein said real time operator comprises means for communicating with said multiprocessor structure according to the following process:
request for access to said real time operator by said structure to process a primitive, with verification beforehand by said structure of free access to said real time operator and subsequent hardware response to said verification from said real time operator to said structure,
if said real time operator is free, sending by said structure of a code and of parameters of the primitive to the real time operator merely by writing an addressing area of the real time operator,
execution by said real time operator after acquisition of said codes and of said parameters of an operating sequence relating to said primitive,
decision by said real time operator, as a function of said primitive and of said real time context:
to produce a response to the processor which requested said primitive,
to interrupt the processors on which said primitive has caused a change of task, and
reading of a real time operator response by the processor which requested said primitive and by the processors which have received an interrupt, at a real time operator address.
4. Device according to claim 3 which comprises a "test and set" type mechanism included in said real time operator which carries out said verification and which is adapted to send to the structure processor which requests access in read mode a response representative of the "free" or "busy" state of said real time operator.
5. Device according to claim 1 wherein said real time operator circuits each allocate according to their own strategy their associated processor to one of their eligible tasks, preferably a task capable of being executed on said processor which has the highest priority.
6. Device for optimizing the performance of a real time executive kernel in a multiprocessor structure comprising one or more processors, said device comprising a real time operator behaving, as seen from a processor of said structure, as a memory area and comprising means for sending and for receiving data to be processed, means for generating communication control signals, means for associating with objects managed by a kernel, especially tasks, each having a state, hardware and software events, resources and time, a series of primitives one primitive at a time to manage a clock resource and active resources, means for managing a real time context of said processors of said structure on the basis of a predetermined strategy by means of a scheduler, said scheduler being adapted in particular to activate the tasks cyclically, means for marking waits on timers, means for activating tasks after timers, and means for deciding to change the state of a task to another state on the basis of the primitives of the real time context, wherein said real time operator is organized in a plurality of identical hardwired real time operator circuits accessible simultaneously by said processors of said structure but each associated with one only of said processors, said circuits being interconnected by a link adapted to transmit an "AGREED" signal ensuring that said real time operator executes only one primitive at a time, each real time operator circuit comprising a scheduler which manages the tasks of only the processor associated with it and global resources and events of the real time operator, said scheduler comprising means for activating the tasks cyclically, means for marking waits on timers and means activating tasks after timers, said real time operator deciding to change the task state on the basis of primitives of the real time context each real time operator circuit comprising at least four automatic devices dedicated to the management of specific real time objects, in particular management of eligible tasks awaiting availability of their processor, management of communications with processors, management of timers, cycles and the real time clock, resource queues, all tasks awaiting an event and processing of external interrupts, said automatic devices communicating with each other via buses internal to said real time operator circuit interconnected by a dynamic router under the control of a sequencer included in one of said automatic devices.
7. Device according to claim 6 wherein said real time operator circuits

are combined on a common circuit board connected to the common bus interconnecting all said processors of said structure with a common interface to said bus.
8. Device according to claim 6 wherein each real time operator circuit is on the circuit board of the processor whose tasks it manages with an interface to the common bus of said multiprocessor structure.
9. Device according to claim 6 wherein each real time operator circuit is colocated with the processor whose tasks it manages with an interface to the local bus so that when a processor of said multiprocessor structure executes a primitive it sends its parameters to the associated real time operator circuit via said local bus and simultaneously to the other real time operator circuits via said common bus and comprises common bus arbiter logic which assures taking possession of said local bus of all said real time operator circuits during a single access.
10. Device according to claim 6 wherein each of said automatic devices comprises a processor unit and at least one input register and one output register and said automatic device outputs and inputs are interconnected by a dynamic router, one or more memory elements in the form of random access memory, for example, and a hardwired sequencer.
11. Device according to claim 10 wherein said real time operator circuit further comprises at least one communication device, possibly an asynchronous communication device, connecting said real time operator circuit and said common bus dedicated interface and means for sending an interrupt signal to the processor concerned only when said operator defines a change of task on said processor after internal processing (timer or hardware event) or after a primitive requested by a processor other than that for which said real time operator circuit is responsible or after a temporal exception (completion time or execution time exceeded, cycle on a task not finished), said interrupt signal remaining active until said processor has accessed said operator to read the code of the operation to be performed.
12. Device according to claim 6 wherein at least one of said automatic devices comprises a real time clock having a period programmable by invoking a specific request to said operator and counting logic.
13. Device according to claim 12 wherein said real time clock is adapted to send an internal interrupt signal to said real time operator circuit initating immediate processing if said real time operator circuit is waiting or after the primitive currently being executed.
14. Device according to claim 6 wherein at least one of said automatic devices comprises external interrupt control inputs and means for shaping and memorizing said interrupt signals which are then routed to a priority encoder and said operator processes the highest priority interrupt stored at this time and resets said memory means.
15. Device according to claim 14 wherein said automatic device managing events further comprises a partially erasable random access memory used when an event occurs to accelerate the clearing of waits on events for all the tasks activated by the event processed.

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CLAIMS:

There is claimed:
1. Device for optimizing the performance of a real time executive kernel in a multiprocessor structure comprising one or more processors, said device comprising a real time operator behaving, as seen from a processor of said structure, as a memory area and comprising means for sending and for receiving data to be processed, means for generating communication control signals, means for associating with objects managed by a kernel, especially tasks, each having a state, hardware and software events, resources and time, a series of primitives one primitive at a time to manage a clock resource and active resources, means for managing a real time context of said processors of said structure on the basis of a predetermined strategy by means of a scheduler, said scheduler being adapted in particular to activate the tasks cyclically, means for marking waits on timers, means for activating tasks after timers, and means for deciding to change the state of a task to another state on the basis of the primitives of the real time context, wherein said real time operator is organized in a plurality of identical hardwired real time operator circuits, accessible simultaneously by said processors of said structure but each associated with one only of said processors, said circuits being interconnected by a link adapted to transmit an "AGREED" signal ensuring that said real time operator executes only one primitive at a time, each real time operator circuit comprising a scheduler which manages the tasks of only the processor associated with it and global resources and events of the real time operator, said scheduler comprising means for activating the tasks cyclically, means for marking waits on timers and means activitating tasks after timers, said real time operator deciding to change the task state on the basis of primitives of the real time context, said device comprising means for commuting each real time operator circuit in one of the following three functioning modes:
a) a first mode in which it processes a primitive requested by one of said processors of said structure,
b) a second mode in which it processes a local request internal to the circuit concerning only tasks for which it is responsible,

Search term used: buffer chip ... and, stim mail, scheduler and multiprocessor.

c) a third mode in which it is awaiting processing.
2. Device according to claim 1 wherein said real time operator comprises means for processing one of said primitives only if all said real time operator circuits are awaiting processing.
3. Device according to claim 1, wherein said real time operator comprises means for communicating with said multiprocessor structure according to the following process:
request for access to said real time operator by said structure to process a primitive, with verification beforehand by said structure of free access to said real time operator and subsequent hardware response to said verification from said real time operator to said structure,
if said real time operator is free, sending by said structure of a code and of parameters of the primitive to the real time operator merely by writing an addressing area of the real time operator,
execution by said real time operator after acquisition of said codes and of said parameters of an operating sequence relating to said primitive,
decision by said real time operator, as a function of said primitive and of said real time context:
to produce a response to the processor which requested said primitive,
to interrupt the processors on which said primitive has caused a change of task, and
reading of a real time operator response by the processor which requested said primitive and by the processors which have received an interrupt, at a real time operator address.
4. Device according to claim 3 which comprises a "test and set" type mechanism included in said real time operator which carries out said verification and which is adapted to send to the structure processor which requests access in read mode a response representative of the "free" or "busy" state of said real time operator.
5. Device according to claim 1 wherein said real time operator circuits each allocate according to their own strategy their associated processor to one of their eligible tasks, preferably a task capable of being executed on said processor which has the highest priority.
6. Device for optimizing the performance of a real time executive kernel in a multiprocessor structure comprising one or more processors, said device comprising a real time operator behaving, as seen from a processor of said structure, as a memory area and comprising means for sending and for receiving data to be processed, means for generating communication control signals, means for associating with objects managed by a kernel, especially tasks, each having a state, hardware and software events, resources and time, a series of primitives one primitive at a time to manage a clock resource and active resources, means for managing a real time context of said processors of said structure on the basis of a predetermined strategy by means of a scheduler, said scheduler being adapted in particular to activate the tasks cyclically, means for marking waits on timers, means for activating tasks after timers, and means for deciding to change the state of a task to another state on the basis of the primitives of the real time context, wherein said real time operator is organized in a plurality of identical hardwired real time operator circuits accessible simultaneously by said processors of said structure but each associated with one only of said processors, said circuits being interconnected by a link adapted to transmit an "AGREED" signal ensuring that said real time operator executes only one primitive at a time, each real time operator circuit comprising a scheduler which manages the tasks of only the processor associated with it and global resources and events of the real time operator, said scheduler comprising means for activating the tasks cyclically, means for marking waits on timers and means activating tasks after timers, said real time operator deciding to change the task state on the basis of primitives of the real time context each real time operator circuit comprising at least four automatic devices dedicated to the management of specific real time objects, in particular management of eligible tasks awaiting availability of their processor, management of communications with processors, management of timers, cycles and the real time clock, resource queues, all tasks awaiting an event and processing of external interrupts, said automatic devices communicating with each other via buses internal to said real time operator circuit interconnected by a dynamic router under the control of a sequencer included in one of said automatic devices.
7. Device according to claim 6 wherein said real time operator circuits

are combined on a common circuit board connected to the common bus interconnecting all said processors of said structure with a common interface to said bus.

8. Device according to claim 6 wherein each real time operator circuit is on the circuit board of the processor whose tasks it manages with an interface to the common bus of said multiprocessor structure.

9. Device according to claim 6 wherein each real time operator circuit is colocated with the processor whose tasks it manages with an interface to the local bus so that when a processor of said multiprocessor structure executes a primitive it sends its parameters to the associated real time operator circuit via said local bus and simultaneously to the other real time operator circuits via said common bus and comprises common bus arbiter logic which assures taking possession of said local bus of all said real time operator circuits during a single access.

10. Device according to claim 6 wherein each of said automatic devices comprises a processor unit and at least one input register and one output register and said automatic device outputs and inputs are interconnected by a dynamic router, one or more memory elements in the form of random access memory, for example, and a hardwired sequencer.

11. Device according to claim 10 wherein said real time operator circuit further comprises at least one communication device, possibly an asynchronous communication device, connecting said real time operator circuit and said common bus dedicated interface and means for sending an interrupt signal to the processor concerned only when said operator defines a change of task on said processor after internal processing (timer or hardware event) or after a primitive requested by a processor other than that for which said real time operator circuit is responsible or after a temporal exception (completion time or execution time exceeded, cycle on a task not finished), said interrupt signal remaining active until said processor has accessed said operator to read the code of the operation to be performed.

12. Device according to claim 6 wherein at least one of said automatic devices comprises a real time clock having a period programmable by invoking a specific request to said operator and counting logic.

13. Device according to claim 12 wherein said real time clock is adapted to send an internal interrupt signal to said real time operator circuit initating immediate processing if said real time operator circuit is waiting or after the primitive currently being executed.

14. Device according to claim 6 wherein at least one of said automatic devices comprises external interrupt control inputs and means for shaping and memorizing said interrupt signals which are then routed to a priority encoder and said operator processes the highest priority interrupt stored at this time and resets said memory means.

15. Device according to claim 14 wherein said automatic device managing events further comprises a partially erasable random access memory used when an event occurs to accelerate the clearing of waits on events for all the tasks activated by the event processed.

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